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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,580	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,11-16,18-22 and 28-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8,11-13,15,16,18-20 and 22-31* is/are rejected.

7)☒ Claim(s) *7, 14, 21 and 32-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/30/2004 has been entered.

Response to Amendment

2. This Office action is in respond to the amendment filed in 08/30/2004.

Specification

3. The disclosure is objected to because of the following informalities:

Page 5 line 6 "the interconnect 265 may include 8 differential pairs, 9 pairs for data, and 9 pairs for address and command." should be -- the interconnect 265 may include 18 differential pairs, 9 pairs for data, and 9 pairs for address and command.--.

Appropriate correction is required.

Claim Objections

4. Claims 1, 3 is objected to because of the following informalities:

Claim 1 lines 7-8, "a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data

cache" is unclear whether both current and next lines are read out from in one of the memory device located in the memory module or both current and next lines are read out from the memory module.

Claim 3 is objected as the same reasons set forth in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 8, 15, 16, 22, and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Shatil et al. (US PAT. 6,278,840 hereinafter Shatil).

Regarding claim 1, Stracovsky disclosures an apparatus, i.e., universal controller (104, figure 1b) comprising an array of tag address storage locations (114, figure 1b), and a command sequencer and serializer unit, i.e., command sequencer (116, figure 1b) coupled to the array of tag address storage locations, the command sequencer and serializer is coupled to memory module (108, figure 1b) to perform the memory transactions requested by the host processor(s) (102, figure 1b), a command sequencer cause a single command, i.e., universal command (200, figure 2a) having a plurality of segments, i.e., data fields, serialized and sequentially transmitted via the memory bus within a single memory access transaction (col. 6 line 50 through col. 8 line

2 and col. 9 line 15 through col. 10 line 34). Stracovsky differs from the claimed invention in not specifically teaches the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines and address lines over a memory bus, the command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device to the data cache. However, Shatil teaches a computer system (100, figure 1) comprising a host pre-fetcher, i.e., memory controller, interacting between the application (112, figure 1), i.e., requestor, and the storage system (150, figure 1), i.e., memory module, wherein a cache (154, figure 1) is located in the storage system, in addition, the host pre-fetcher comprising a pre-fetch lookup process (212, figure 2) and pre-fetch database (220, figure 2) corresponding to the cache (154, figure 1) in the storage system, i.e., tag array look-up corresponding to the address in the memory module, in addition, Shatil teaches the host pre-fetcher in able to generate pre-fetch command based upon the request from the application (112), which pre-fetch the related data corresponding to the request, and stored in the cache (154) via the command buses (140 and 135, figure 2) and (col. 13 line 49 through col. 16 line 47 and figure 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory controller of Stracovsky in having the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines and address lines over a memory bus, the command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device to the data cache, as per teaching by Shatil, because it eliminates conventional cache management problems such as caching delay, caching unnecessary data and problems do to file

fragmentation, and significantly increase the optimal use of cache memory systems within data storage systems which thereby increases overall data storage system performance.

Regarding claim 3, Shatil disclosures the apparatus wherein the single command, i.e., request from application (112) comprises a read and preload command delivered to the data cache (154) located on the memory module (150), the read and preload command to cause the current line of data to be read out of the memory module memory device and to load the next line of data, i.e., related data, from the memory module memory device to the data cache (col. 13 line 49 through col. 16 line 47 and figure 7).

Regarding claim 8, Stracovsky discloses a memory module (108, figure 1b), comprising at least one memory device (device type1 – device type N, figure 1c), and the memory controlled by a memory controller, i.e., universal controller (104, figure 1b) via a memory bus (220, figure 1b), the memory controller component including an array of tag address storage locations, i.e., resource tags (114, figure 1b). Stracovsky differs from the claimed invention in not specifically teaches the memory module comprising a data cache coupled to the memory device, the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out of the command device and to load a next line of data from the memory device to the data cache. However, Shatil teaches a computer system (100, figure 1) comprising a host pre-fetcher, i.e., memory controller, interacting between the application (112, figure 1), i.e., requestor, and the storage system (150, figure 1), i.e., memory module, wherein a cache (154, figure 1) is located in the storage system, in addition, the host pre-fetcher comprising

a pre-fetch lookup process (212, figure 2) and pre-fetch database (220, figure 2) corresponding to the cache (154, figure 1) in the storage system, i.e., tag array look-up corresponding to the address in the memory module, in addition, Shatil teaches the host pre-fetcher in able to generate pre-fetch command based upon the request from the application (112), which pre-fetch the related data corresponding to the request, and stored in the cache (154) via the command buses (140 and 135, figure 2) and (col. 13 line 49 through col. 16 line 47 and figure 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache coupled to the memory device, the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out of the command device and to load a next line of data from the memory device to the data cache, because it eliminates conventional cache management problems such as caching delay, caching unnecessary data and problems do to file fragmentation, and significantly increase the optimal use of cache memory systems within data storage systems which thereby increases overall data storage system performance.

Regarding claim 15, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller, i.e., universal controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B) he memory controller including an array of tag address storage locations (114, figure 1B), and command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations as defined in figure 1, a

memory module (108, figure 1B) coupled to the memory controller via a memory bus (220, figure 1B), the memory module including at least one memory device (device type 1 – device type N, figure 1C). Stracovsky differs from the claimed invention in not specifically teaches the memory module including a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, one of the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction to cause a current line of data to be read out of the memory device and to load a next line of data from the memory device to the data cache. However, Shatil teaches a computer system (100, figure 1) comprising a host pre-fetcher, i.e., memory controller, interacting between the application (112, figure 1), i.e., requestor, and the storage system (150, figure 1), i.e., memory module, wherein a cache (154, figure 1) is located in the storage system, in addition, the host pre-fetcher comprising a pre-fetch lookup process (212, figure 2) and pre-fetch database (220, figure 2) corresponding to the cache (154, figure 1) in the storage system, i.e., tag array look-up corresponding to the address in the memory module, in addition, Shatil teaches the host pre-fetcher in able to generate pre-fetch command based upon the request from the application (112), which pre-fetch the related data corresponding to the request, and stored in the cache (154) via the command buses (140 and 135, figure 2) and (col. 13 line 49 through col. 16 line 47 and figure 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache coupled to the memory device, the plurality of commands including a read and preload command, as a single

command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out of the command device and to load a next line of data from the memory device to the data cache, because it eliminates conventional cache management problems such as caching delay, caching unnecessary data and problems do to file fragmentation, and significantly increase the optimal use of cache memory systems within data storage systems which thereby increases overall data storage system performance.

Regarding claim 16, Stracovsky disclosures the system wherein the memory module further includes a command decoder and deserializer unit to receive command and address information from the memory controller, i.e., processor, the command decoder and deserializer unit providing control for the data cache (col. 15 line 23 through col. 26).

Regarding claim 22, Stracovsky disclosures the system further comprising a point-to-point interconnect to couple the memory controller to the memory module (figure 9a).

Regarding claims 28-29, Stracovsky disclosures the apparatus wherein each of the segments, i.e. command components (202-210) of the universal command received from the processor(s) (102, figure 1b) is transmitted within one of the transfer periods over one of the command and address lines, a segment of the command transmitted in a last transfer period of a command line includes information indicating a cache hit (col. 6 line 50 through col. 8 line 2 and col. 9 line 16 through col. 10 line 34).

Regarding claim 30, Stracovsky disclosures the apparatus wherein a segment of the command transmitted in a last transfer period of a command line includes information implicating a cache way of the data cache on a memory module (col. 8 lines 3-32).

Regarding claim 31, Stracovsky disclosures the apparatus wherein a segment of the command transmitted in a last transfer period of a command line includes eviction information of an eviction buffer of the data cache (col. 6 line 50 through col. 8 line 2 and col. 9 line 16 through col. 10 line 34).

7. Claims 4-6, 11-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,718 hereinafter Stracovsky) and Shatil et al. (US PAT. 6,278,840 hereinafter Shatil) further in view of Ayukawa et al. (US PAT. 6,381,671 hereinafter Ayukawa).

Regarding claim 4, the combination of Stracovsky and Shatil differs from the claimed invention in not specifically teaches the read and pre-load command includes memory module destination information, cache way information, address strobe state information and cache hit information. However Ayukawa teaches such (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of the combination of Stracovsky and Shatil in having the read and pre-load command including memory module destination information, way information, address strobe state information and cache hit information, as per teaching by the system of Aynkawa, because it enhances the hit ratio of the sense amplifier cache by next address self-prefetching, and enhances the speed of first access to a multi-bank memory.

Regarding claim 5, Ayukawa discloses the read and preload command further includes column address information and memory device bank information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claim 6, Ayukawa discloses the read and preload command information delivered over four transfer periods within a single memory access ransaction, i.e., 6 to 8 clock cycles (figure 6 and 7 and col. 13 line 47 through col. 15 line 4).

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 13, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Allowable Subject Matter

8. Claims 7, 14, 21 and 32-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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